A Continuously Adjustable Video-Frequency Current Amplifier for Filter Applications

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Abstract

The adjustable balanced-signal current amplifier presented in this paper amplifies a current by first transforming it into a voltage signal using two poly-silicon resistors and then back into a current signal using a single MOSFET resistor operating in the linear region. We implemented the amplifier in the double-poly 0.6 µm CMOS process by Austria Mikro Systeme International. It consumes 12.4 mW from a 3.3 V supply and covers an area of 0.07 mm^2. Measurements show that it is suitable for building biquadratic filters with a spurious-free dynamic range of more than 45 dB, a pole Q of 3 and a pole frequency of up to 900 kHz. We also show that a modification of the circuit allows building filters with pole frequencies up to 6 MHz.

1 Introduction

Our motivation for building an adjustable current amplifier, called current-controlled current source (CCCS) in this paper, is the integration of single-amplifier biquadratic filters (SABs) in CMOS, to be used, for example, as video-frequency anti-aliasing filters on the same chip with sampled-data systems.

The low-gain amplifier needed for building Sallen-Key SABs is normally implemented as a high-gain voltage amplifier (opamp) with negative feedback. The feedback stabilizes the gain and reduces harmonic distortion and output resistance by a factor proportional to the feedback loop gain. However, a lowpass filter can still operate properly if its f_p is so close to the opamp's unity-gain frequency that the open-loop gain is only about five. Then the stabilization is no longer very effective, and using open-loop low-gain amplifiers becomes attractive: the resulting filter will consume less power, but will also be slightly less linear.

In a Sallen-Key lowpass filter, the pole frequency f_p depends only on the geometric means of the resistors and capacitors, while its pole quality factor q_p depends only on the component spreads and the amplifier gain [2]. Because of the notoriously low precision of absolute component values on CMOS ICs,[1] some of the passive components *must be adjustable* to tune the pole frequency of the filter. This is why such filters are built as MOSFET-C rather than RC filters. We chose to use current amplifiers and build current-mode MOSFET-C filters because very fast low-gain open-loop amplifiers can be built by combining a low-impedance input stage with a low-gain stage consisting of current mirrors [2]. As usual in MOSFET-C filters, a differential-input balanced-output current amplifier is required such that the even-order nonlinearities of the MOSFET resistors are cancelled [2–4].

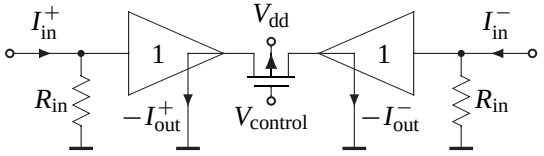

Figure 1: Adjustable Current Amplifier: Concept.

It was shown in [2] that a filter with $q_p = 3$ and a standard deviation $\sigma_{q_p} = 3\,\%$ can be readily implemented in CMOS. If this is not precise enough, it is either necessary to tune the component spread of the MOSFET resistors as well, which makes the tuning circuitry very complicated, or the gain of the current amplifier, which makes it necessary to implement an adjustable CCCS.

In this paper, we discuss the implementation of a CCCS whose gain can be adjusted by controlling the gate voltage of a single MOSFET resistor. Compared to other implementations with more complicated adjustable resistors (c.f. [5]), our amplifier is faster at the same power consumption, but also less linear.

We will now present design and measurements of a test circuit built using the 0.6 µm double-poly CMOS process by Austria Mikro Systeme International, and we will show that it is possible to build a 6 MHz filter with $q_p = 3$ and a spurious-free dynamic range of 45 dB using this process and our amplifier.

2 Circuit Description

The concept of our adjustable CCCS is shown in Fig. 1. The input current I_{in}^{+} flows through a poly-silicon resistor R_{in}. The resulting voltage is buffered with unity gain. The same happens with I_{in}^{-}. The voltage difference over the MOSFET resistor causes a current to flow out of one voltage buffer and into the other. Both currents are sensed and mirrored to high-impedance outputs. The overall current gain can then be adjusted almost linearly by varying the control voltage of the MOSFET resistor.

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[1] Poly-silicon resistors can easily have a standard deviation of 20 % or more.

The idea of implementing a transconductance amplifier by connecting two voltage buffers to a simulated resistor was presented in [5], but there a six-transistor resistor was used. We show in this paper that using a single MOSFET resistor is sufficient, provided that the input signal is in differential mode. A pure differential-mode voltage signal applied to a strongly inverted MOSFET in the linear region will theoretically cause a distortion-free channel current [6]. Any common-mode signal will be rejected almost completely, since it is the voltage *difference* which is converted into a current. However, simply stating that the common-mode rejection ratio is very high would be misleading, since a common-mode signal changes the resistance of the MOSFET resistor and therefore *modulates the amplitude of the differential-mode signal.*

We had to use pMOS resistors in our 3.3 V design, because in the AMS 0.6 µm process, the nMOS transistors have the larger body effect constant γ. This causes the nMOS channel to be less strongly inverted than the pMOS channel, which increases both the standard deviation of the MOSFET resistance and the harmonic distortion.

It is also advantageous to make the voltage difference between the MOSFET's gate and channel as large as possible. One way to do this is to choose the operating point voltage of the voltage buffer outputs above analog ground (agnd, in our design the voltage in the middle between the rails). Therefore a voltage buffer with voltage level shift must be used. We chose the same buffer that was used in [5]; it is shown in Fig. 2.

The operation of the circuit in Fig. 2 is fairly straightforward. Transistor M 43 is biased with a constant current I_{bias}. This makes its gate-source voltage approximately constant as well, and it acts as voltage buffer with a voltage level shift of approximately 1.25 V in our implementation. Any current flowing through the terminal 'V_{out}' is conducted by M 53, which is also biased with I_{bias}. This current is then mirrored by M 13 and provided at the high-impedance output 'I_{out}'.

The same voltage buffer is used a second time in the circuit, namely to provide the signal ground to which R_{in} is connected. Connecting it directly to the analog-ground ('agnd') line on the chip would be a bad idea, since the signal current injected into that line would cause a voltage drop at the bonding wires. As a result, the 'agnd' line would bounce and feed interference into every other component on the chip using analog ground as a reference voltage. The adjustable CCCS therefore consists of four voltage buffers, fourteen constant current sources providing the currents I_{bias}, two current mirror output stages and a single MOSFET resistor.

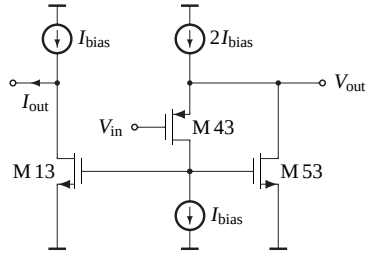


Figure 2: Voltage buffer with level shift.

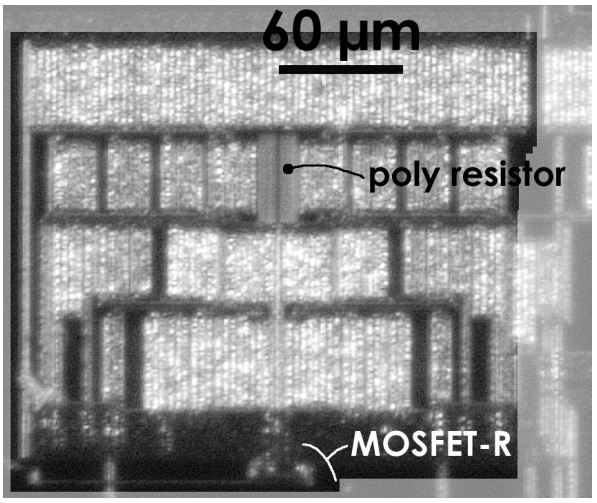


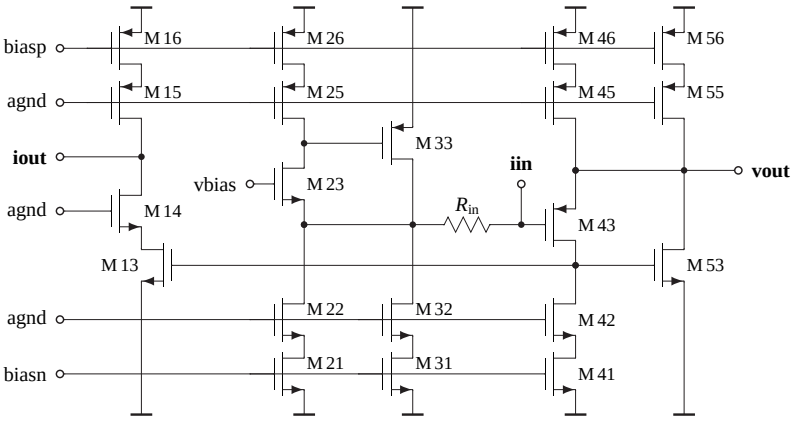
Figure 3: Chip photo.

The schematic of the half-circuit is shown in Fig. 4. The bias voltage applied to 'vbias' is buffered, with a negative level shift, by the first voltage buffer M [2,3][1–6].[2] M 23 provides the voltage buffering function, M 33 collects the current applied to 'iin', and the other transistors form constant current sources, all supplying the same current I_{bias}. The voltage drop over the poly-silicon resistor R_{in} is then copied to 'vout', the terminal connected to the MOSFET resistor, by the voltage buffer M [4,5][1–6] from Fig. 2. M 1[3–6] form a class A current mirror together with M 53. Since the drain voltage of M 13 is always lower than the drain voltage of M 53, the former is made a bit wider than the latter to compensate for systematic offset.

We biased all cascode transistors by analog ground, which results in an output voltage swing sufficiently large to build MOSFET-C filters [2]. The voltage applied to 'vbias' is approximately 1.1 V above analog ground and sets both the signal ground at the current input and the operating point voltage at the MOSFET resistor's terminals, which is about 1.2 V above 'agnd' in our implementation.

The circuit described above was implemented using the AMS 0.6 µm process. A chip photo of the full CCCS is shown in Fig. 3. Its area, including interconnections, bias circuits and an empty 5 µm perimeter around everything, is only 0.07 mm^2.

[2] M[2,3][1–6] denotes all transistors whose first digit is a 2 or a 3, and whose second digit is in the range 1–6.



Transistor	Dimensions
M [2–4]1	$100 \times 1.8\,\mu$m
M [2–4]2	$96 \times 0.6\,\mu$m
M 13	$130.8 \times 1.8\,\mu$m
M [2,5]3	$126 \times 1.8\,\mu$m
M [3,4]3	$200.1 \times 1.2\,\mu$m
M 41	$120 \times 0.6\,\mu$m
M [1,2,4,5]5	$224 \times 0.6\,\mu$m
M [1,2,4,5]6	$300 \times 1.8\,\mu$m
MOSFET-R	$12 \times 3\,\mu$m

$R_{\text{in}} = 12.46\,\text{k}\Omega$

$I_{\text{bias}} = 375\,\mu\text{A}$

Figure 4: Adjustable Current Amplifier: Half-Circuit Schematic.

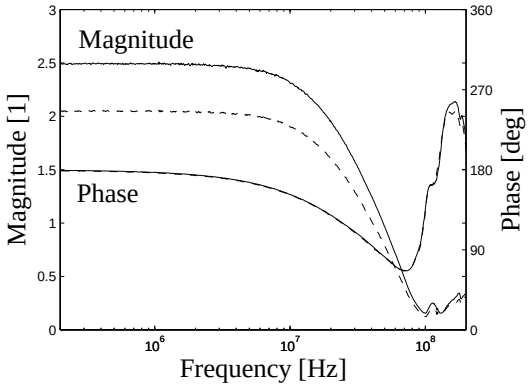


Figure 5: Measured transfer function for $V_{\text{control}} = -1.65\,\text{V}$ and $V_{\text{control}} = -1.30\,\text{V}$ (dashed).

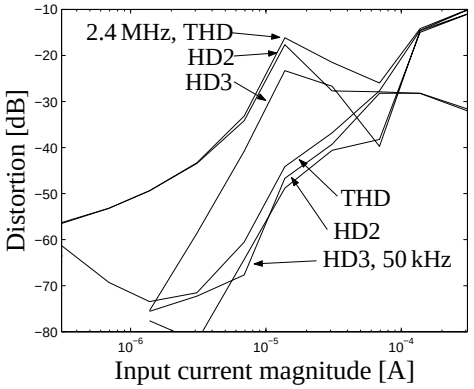


Figure 6: Distortion measurements: THD, HD 2 and HD 3 measured at 50 kHz and 2.4 MHz.

3 Measurement Results and Discussion

The measurement results presented in this section show that the CCCS on the test chip has too low a spurious-free dynamic for building biquadratic filters with a pole frequency higher than 1 MHz. The reason is that the output resistance of the voltage buffer driving the MOSFET resistor is too high. We will demonstrate, however, that much can be gained through using a more elaborate voltage buffer with a lower output resistance, through two effects: First, this makes the two balanced signal paths match better, which reduces mainly the second-order harmonic distortion (HD 2). Second, the transfer characteristic generally becomes more linear, which reduces all odd-order harmonic distortion.

The transfer function of the CCCS is shown in Fig. 5 for two control voltages. In between them, the DC gain can be tuned almost linearly from 2.1 up to 2.5 without affecting the phase of the transfer function, which is more than enough to tune q_{p}. The phase lag reaches -30 degrees at 12 MHz, which is therefore approximately the maximum frequency at which an SAB can reasonably be expected to operate [1].

Figure 6 shows the measured second-order (HD 2), third-order (HD 3) and total harmonic distortion (THD) for frequencies of 50 kHz and 2.4 MHz. The latter frequency is one fifth of the 12 MHz mentioned above, which is where the THD of a lowpass filter is conventionally measured. It is obvious that the 2.4 MHz curve is dominated by second-order harmonic distortion, indicating that the two balanced paths match very badly. If a low-output-resistance voltage buffer is used, the two paths match much better, and the second-order harmonic distortion decreases considerably.

Using a voltage buffer with local feedback having a low output resistance R_{out} also makes the output characteristic more linear, which can be seen in Fig. 7. This figure shows the measured THD (at 50 kHz), and the THDs calculated from simulated DC characteristics.[3] The calculated and measured curves agree very well. It can also be seen that the low-R_{out} curve raises at much higher current levels, and raises steeper, which indicates that the remaining distortion is essentially caused by clipping when the signal current comes close to the

[3]Note that the "noise" in the simulated curves is an artefact caused by round-off errors of the programme calculating the THD.

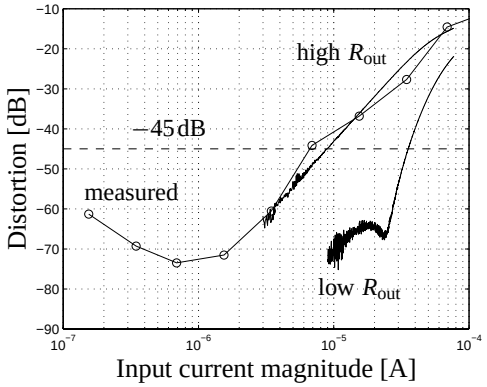


Figure 7: Measured and simulated THD (see text).

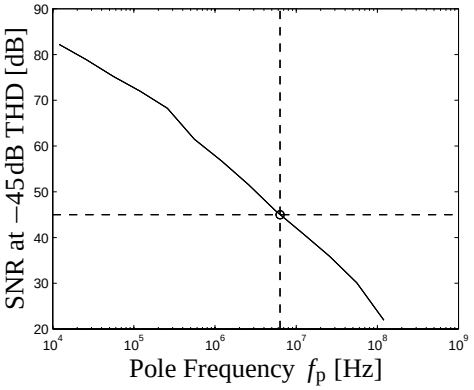


Figure 8: SNR in function of f_p for $q_p = 3$.

MOSFET resistor's saturation current. At the distortion level of −45 dB required for most video applications, the maximum possible input signal magnitude increases from 9 µA to 36 µA, or by 12 dB, when a low-R_{out} voltage buffer is used.

The noise in the CCCS is mainly caused by the active elements, the resistors do not matter. In video-frequency circuits, the measured spectral density of the equivalent white-noise input current, $i_{nin} = 14\,\mathrm{pA}/\sqrt{\mathrm{Hz}}$, clearly dominates the $1/f$-noise. The noise power and the spurious-free dynamic range then depend on the specific filter built using this amplifier.

For example, the noise bandwidth of a second-order lowpass filter is $\pi/2 \cdot q_p \cdot f_p$. The spurious-free dynamic range is defined as the point where the noise-to-signal ratio (NSR) is equal to the total harmonic distortion (THD), where the latter is conventionally measured at $f_p/5$.

The maximum possible pole frequency of a filter with $q_p = 3$ to guarantee a spurious-free dynamic range of −45 dB is slightly above 900 kHz. The use of a low-R_{out} voltage buffer makes it possible to build a 6 MHz filter, a frequency which was estimated by applying the discussion above: For every pole frequency f_p, measure the total harmonic distortion at $f_p/5$ and subtract the second-order distortion to account for the better matching. Determine the signal magnitude causing −45 dB of harmonic distortion and multiply it by 12 dB to account for the increase of the maximum signal current. Finally, divide this value by $\sqrt{2}$ times the RMS value of the white noise inside the filter's noise bandwidth to obtain the signal-to-noise ratio. The resulting curve is shown in Fig. 8. It can be seen that the maximum possible pole frequency with an SFDR of 45 dB or more is $f_p = 6.3$ MHz.

This is about the maximum frequency which can be reached using AMS's 0.6 µm process if the gate-bulk voltage of the MOSFET resistor is restricted to 3.3 V. To increase this frequency, either the supply voltage of the filter must be increased, or an nMOS resistor must be used whose control voltage is brought above the positive rail by a charge pump.

4 Conclusions

The adjustable, balanced-signal CCCS presented in this paper can be used to build video-frequency filter up to pole frequencies of about 6 MHz with a spurious-free dynamic range of 45 dB or more. It is small (0.07 mm^2) and power-efficient (it consumes only 12.4 mW). However, we conclude from the discussion above that a pole frequency of 6 MHz can probably not be exceeded with the 0.6 µm double-poly CMOS process by Austria Mikro Systeme International. This is still far below what is possible with this process (c.f. the 24 MHz MOSFET-C lowpass filter in [2]). If the filter frequency should be pushed towards the physical limits without increasing the supply voltage, a fixed-gain amplifier must be used and the MOSFET resistor spreads must be tuned, as mentioned in the introduction.

References

[1] Hanspeter Schmid and George S. Moschytz, "Fundamental frequency limitations in current-mode Sallen-Key filters," in *Proc. ISCAS*, Monterey, California, June 1998, vol. 1, pp. 57–60.

[2] Hanspeter Schmid and George S. Moschytz, "A tunable, video-frequency, low-power, single-amplifier biquadratic filter in CMOS," in *Proc. ISCAS*, Orlando, Florida, June 1999.

[3] Mihai Banu and Yannis Tsividis, "Fully integrated active RC filters in MOS technology," *IEEE J. Solid-State Circuits*, vol. 18, no. 6, pp. 644–651, Dec. 1983.

[4] Mihai Banu and Yannis Tsividis, "Detailed analysis of nonidealities in MOS fully integrated active RC filters based on balanced networks," *IEE Proc., pt. G*, vol. 131, no. 5, pp. 190–196, Oct. 1984.

[5] Tom Kwan and Kenneth Martin, "An adaptive analog continuous-time CMOS biquadratic filter," *IEEE J. Solid-State Circuits*, vol. 26, no. 6, pp. 859–867, June 1991.

[6] Yannis Tsividis, Mihai Banu, and John Khoury, "Continuous-time MOSFET-C filters in VLSI," *IEEE J. Solid-State Circuits*, vol. 21, no. 1, pp. 15–30, Feb. 1986.