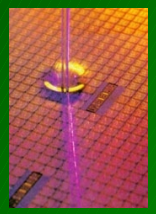

A Tunable, Video-Frequency, Low-Power, Single-Amplifier Biquadratic Filter in CMOS

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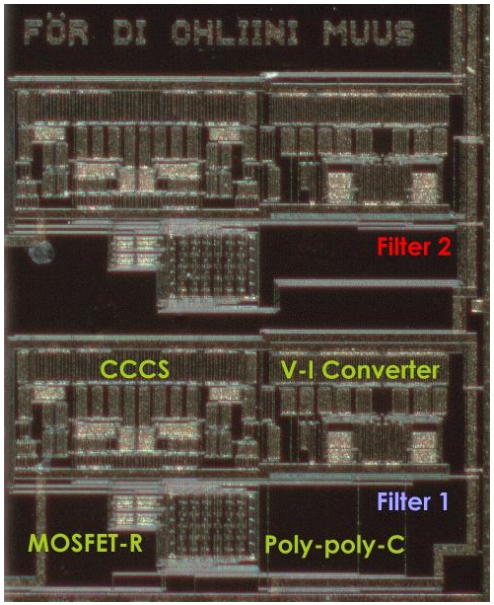
Introduction

Why single-amplifier biquadratic filters? They need only one amplifier per complex pole pair. Compared to integrator-connected topologies (*at least* one amplifier *per pole*), they consume less power, but their pole quality factor is also more sensitive to variations of the passive component values and the amplifier gain.

Why current-mode? The question should actually be "why not use a high-gain amplifier with negative feedback?" Feedback makes the closed-loop gain more precise and reduces both the input resistance of the amplifier's low-impedance terminals and the harmonic distortion. Pushing the pole frequency as far up as possible, one finds that an SAB with a pole frequency of one fifth of the amplifier's gain-bandwidth product still operates properly. There the loop gain is less than five, and the stabilization is no longer very effective. Thus we chose an open-loop amplifier in the first place, and we found it easier to build such an amplifier in current-mode.

How good is the filter? It operates from a 3.3 V supply, consumes 2.4 mW per pole at a pole freqency of 24 MHz and a pole-Q of 3 and covers an area of 0.06 mm^2 per pole. The inter-chip matching is very good with 1.5 % and 3 % standard deviation of pole frequency and pole quality factor, respectively. A spurious-free dynamic range of 45 dB, as required for many video-frequency applications, can be achieved if a simple modification is made to the filter (see fourth column).

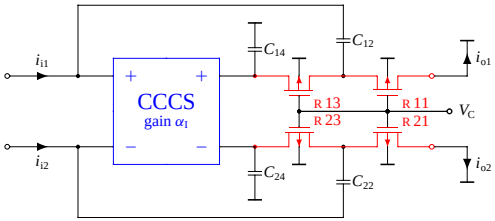


Chip Microphotograph: Two "Identical" Lowpass Filters

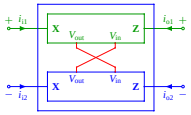
Circuit Description

This filter is derived from an active-RC second-order Sallen-Key lowpass filter by replacing the resistors by MOSFETs operating in the linear region. The passive network is connected to a balanced-signal current-controlled current source (or current conveyor) with gain −2.6, such that most of the even-order harmonic distortion is cancelled when the signal difference is taken at the output.

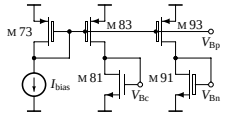
Note: Transistors with box gates are actually simple cascodes (→ paper).



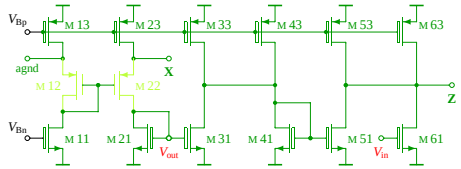
Active-MOSFET-C Second-Order Lowpass Filter



Block Diagramm of the CCCS



Bias Circuit

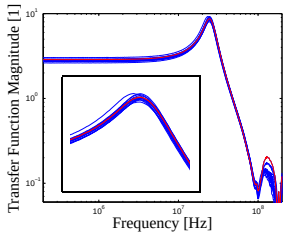


Circuit Schematic of the CCCS Half Circuit

	Main Transistors	Cascode Trans.
M [1–4]1	45 × 3 µm	80 × 0.6 µm
M [5–6]1	57.3 × 3 µm	104 × 0.6 µm
M 81	37.3 × 3 µm	—
M 91	45 × 3 µm	80 × 0.6 µm
M [1–2]2	120 × 0.6 µm × 2	—
M [1–4]3	120 × 3 µm	200 × 0.6 µm
M [5–6]3	200 × 3 µm	260 × 0.6 µm
M [7–9]3	120 × 3 µm	200 × 0.6 µm
R [1–2]1	22 × 2.4 µm × 2	—
R [1–2]2	22 × 1.9 µm × 2	—
C [1–2]2	13.6 × 13.6 µm × 10 (1.0 pF)	—
C [1–2]4	13.6 × 13.6 µm × 1 (0.1 pF)	—

Capacitor and Transistor Dimensions

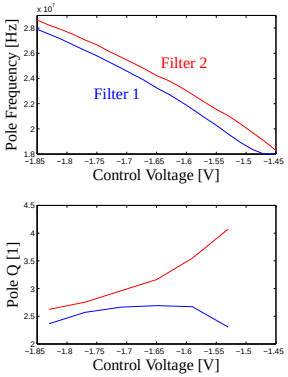
Transfer Function Measurement



Transfer Functions of Filter 2 on all 14 Chips

For Filter 2, measurements and simulations of the extracted layout using BSIM 3v3 models agree very well. The red curve is the filter on Chip 13, which was used for distortion and noise measurements because its pole frequency and quality factor are close to the mean values of 24.2 MHz and 3.07, respectively.

Note: All measurements on this poster were made with an off-chip I–V converter and voltage difference amplifier. The filter's outputs were both loaded with 750 Ω, as they would be in a filter cascade.



Pole Frequency and Pole Q, Filters 1 and 2

Matching

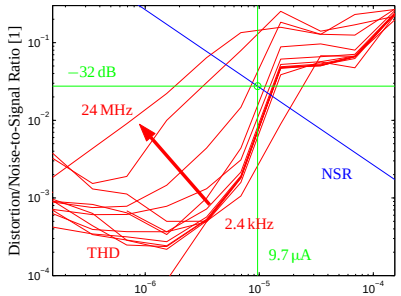
On-chip Matching: The two "identical" filters on the chip are not really identical. In Filter 1, the supply of the filter and of the on-chip V–I converter are split, and the layout of the signal lines is different. As a consequence, both pole frequency and pole Q are much lower than simulated.

Inter-chip Matching: For both Filter 1 and 2, the standard deviations are 1.5 % and 3 % for pole frequency and pole quality factor, respectively. We believe that an on-chip pole-frequency matching better than 1 % can be achieved if the layouts of the signal lines are the same in both filters.

Noise and Distortion Measurement

To determine the spurious-free dynamic range (SFDR) of our circuit, we measured noise and harmonic distortion. The output noise was calculated as the RMS value of the measured white noise floor of the amplifier times the square root of the filter's noise bandwidth, $\pi/2 \cdot q_p\, f_p$. The noise of the measurement circuitry was then subtracted. The total harmonic distortion is the sum of the second to fifth harmonics generated by a sine input signal and *includes* the distortion caused by the measurement circuits. It is shown over four decades of frequency, with three steps per decade.

The green circle in the following figure marks where the NSR curve would intersect the THD curve for 4.8 MHz, which is $f_p/5$ (not shown, but close to the 5.2 MHz curve left of the green circle). The maximum possible input current magnitude of 9.7 µA is only 6 % of the input stage's bias current, meaning that there is much room to increase the SFDR of only 32 dB.



Total Harmonic Distortion and Noise-to-Signal Ratio

Discussion and Conclusions

Why is the test filter off the mark? We actually designed the filter for a pole frequency of 17 MHz. Unfortunatley, the BSIM 3v2 models then available are unsuitable for designing MOSFET-C circuits, so we obtained pre-release BSIM 3v3 models. Nevertheless, when the circuit came back, it had a pole frequency of 24 MHz instead of 17 MHz and had more harmonic distortion than anticipated.

The official BSIM 3v3 models released after the fabrication of the chip agree very well with the measurements. Using these models, a filter with the correct SFDR of 45 dB can easily be designed.

How can an SFDR of 45 dB be achieved? The maximum possible input signal must be 13 dB larger (by a factor of 4.46), or approx. 45 µA. Since the limiting factor is really the saturation current of the MOSFET resistors, the SFDR can be increased by moving the internal signal ground towards the positive rail and re-sizing the MOSFETs at the same time to maintain the same resistance. Simulations showed that the maximum achievable input signal will be above 50 µA, which means that an SFDR of 45 dB can certainly be achieved. Furthermore, since this current is still not large compared to the input-stage bias current of 160 µA, a redesign of the CCCS is not necessary.